TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0696US

In Re Application Of: **David A. Kiss**

Serial No.	Filing Date	Examiner	Group Art Unit
10/017,031	**October 30, 2001**	**Sheila Clark**	**2815**

Invention: **Packaged Combination Memory for Electronic Devices**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **January 22, 2003.**

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Dated: **February 18, 2003**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant: David A. Kiss	§	Art Unit:	2815
Serial No.: 10/017,031	§	Examiner:	Sheila Clark
Filed: October 30, 2001	§		
For: Packaged Combination Memory for Electronic Devices	§	Atty Docket:	ITL.0696US P13281

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APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed October 22, 2002.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

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II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claims 1-24 are rejected. Each rejection is appealed.

Date of Deposit: February 18, 2003
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IV. STATUS OF AMENDMENTS

Any amendments were entered.

V. SUMMARY OF THE INVENTION

Referring to Figure 1, a packaged integrated circuit device 10 may include a bus 12 that couples a plurality of memories of different memory types to a processor 14. By combining a plurality of different types of memory within the same package with a processor 14, a solution may be provided to the varying memory needs of a wide variety of portable device equipment manufacturers.

A cross-point memory 16 may be a polymer memory and may primarily be utilized for mass storage of data. A volatile memory 22 may be provided for cache and frequent write functions. A phase-change memory 18 may be utilized for both data and code storage needs and a non-volatile memory 20 may also be provided for code storage purposes.

The polymer memory involves polymer chains with dipole moments. Data may be stored by changing the polarization of a polymer between conductive lines. For example, a polymeric film may be coated with a large number of conductive lines. A memory location at a cross-point of two lines is selected when the two transverse lines are both charged. Because of this characteristic, polymer memories are one type of cross-point memory. Another cross-point memory being developed by Nantero, Inc. (Woburn, MA) uses crossed carbon nanotubules.

Cross-point memories are advantageous since no transistors are need to store each bit of data and the polymer layers can be stacked to a large number of layers, increasing the memory capacity. In addition, the polymer memories are non-volatile and have relatively fast read and write speeds. They also have relatively low costs per bit and lower power consumption. Thus,

the polymer memory has a combination of low cost and high capacity that fits well in handheld data storage applications.

The memories 16, 18, 20 and 22 may be integrated within the same integrated circuit package as separate dice in one embodiment of the present invention. In one embodiment of the present invention, the bus 12 may be integrated in the same die with the processor 14. Thus, each of the dice containing the memories 16, 18, 20 and 22 may be electrically coupled to a die including the processor 14 and the bus 12 in accordance with one embodiment of the present invention. For example, the dice containing the memories 16, 18, 20 and 22 may simply be stacked over a die containing the processor 14 and bus 12 and then the dice may be encapsulated within the same package 10. See specification at page 4, line 23 through page 5, line 23.

By encapsulating the various memory types within a single package 10 with the processor 14, a solution may be provided to virtually any memory need of any portable device. Thus, portable device manufacturers may simply use the package 10 and may be assured that a complete solution is available for all their memory needs. This may improve the standardization of portable devices and, as a result, may reduce costs.

VI. ISSUES

A. Is Claim 1 Obvious Over Haba in View of Mauritz, Hsuan, and Kim?

B. Is Claim 10 Obvious Over Haba in View of Mauritz, Hsuan, and Kim?

C. Is Claim 18 Obvious?

VII. GROUPING OF THE CLAIMS

For convenience on appeal:

A. Claims 2-9 may be grouped with claim 1;

B. Claims 11-17 may be grouped with claim 10; and

C. Claims 19-24 may be grouped with claim 18.

VIII. ARGUMENT

A. Is Claim 1 Obvious Over Haba in View of Mauritz, Hsuan, and Kim?

Claim 1 calls for a circuit that is packaged and includes a processor, a volatile memory, and a cross point memory. Clearly and indisputably, the Mauritz patent does not teach a packaged structure. Mauritz is explicit for example, in the figure on the first page, that different chips 24, 26, 22, and 12 are used. There is no indication of an intent to package the disparate memory elements into the same package.

None of the cited references teach the combination within a package of a processor and the two different types of memory. No where is a single packaged part capable of implementing the complete solution set forth in claim 1. Mauritz certainly teaches away from putting all the components in one package and, rather, teaches a conventional non-integrated, non-packaged, computer system. All that Haba suggests is a packaged integrated circuit with a processor and memory die. There is nothing in Haba that suggests the complete solution claimed.

With the single package solution, a one packaged component solves all problems approach may be provided. In other words, regardless of the application, a single packaged integrated circuit may be supplied and may be able to handle essentially any type of memory application. Packaging all of these different functionalities into the same package is no where suggested in Mauritz.

Such a packaged device could effectively provide complete solutions for processor-based system applications. For example, the volatile memory can temporarily store data that is permanently stored in a cross point memory. In some cases no mechanical memory, such as a hard disk drive, need be provided. Thus, the combination of the three elements inside one package provides an advantageous solution.

The single packaged product could provide essentially any memory need that any processor-based system might have. Namely, the combination of a volatile memory with a cross point memory provides an effective memory system for a processor-based system. See e.g., the specification at page 5, line 24 though page 6, line 5. Particularly, in the case of portable processor-based systems, the system set forth in claim 1 would be particularly advantageous.

Even if it is assumed that Mauritz's CPU 12 has an integral ROM memory, this does not teach a packaged device that includes a volatile memory since a ROM is not a volatile memory and it certainly does not teach a packaged device that includes a cross point memory.

With respect to the argument that hundreds of chips may be packaged together, even if this is so, and even if it is intended to refer to dice by the word chips, it still does not teach packaging the particular claimed elements together as claimed.

Failing the teaching anywhere in the prior art of the complete solution claimed or a rationale to modify the references to teach that solution, the claimed invention is non-obvious. Merely the fact that someone teaches a variety of memory devices to be packaged together with a processor does not teach the specific combination within one package of a processor, a volatile memory, and a cross point memory.

Therefore, the rejection of claim 1 should be reversed.

B. Is Claim 10 Obvious Over Haba in View of Mauritz, Hsuan, and Kim?

Claim 10 calls for providing a processor and a cross point memory on separate dice and packaging those dice in the same package. The office action argues that Haba shows a packaged integrated circuit comprising a processor and memory die. It is not contended, nor could it be, that Haba teaches packaging a cross point memory and processor on separate dice within the same package. Nothing in any of the references teach the specific combination of a processor and a cross point memory within the same package.

While it may be advantageous to put a number of dice in the same package, nothing in the prior art suggests the specific combination of a processor and a cross point memory being combined in this way.

The argument that Haba inherently utilizes the steps of providing coupling and packaging simply misreads the claim. The claim calls for providing a cross point memory and a processor on separate dies and packaging those devices in the same package. No such teaching is anywhere found within the cited reference. If anything, Mauritz teaches away because it teaches separately packaged processors and cross point memories.

Therefore, the rejection of claim 10 should be reversed.

C. Is Claim 18 Obvious?

Claim 18 calls for a packaged integrated circuit in which the processor and the cross point memory are on separate dice within the integrated circuit package. Certainly this is no where suggested in any of the cited references.

IX. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: 2/18/03

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APPENDIX OF CLAIMS

The claims on appeal are:

1. A packaged integrated circuit comprising:

a processor;

a volatile memory; and

a cross-point memory.

2. The circuit of claim 1 including a first die and a second die, wherein said processor is on said first die and said cross-point memory is on said second die.

3. The circuit of claim 2 wherein said first die includes a processor and a bus that couples said processor to the volatile memory and the cross-point memory.

4. The circuit of claim 1 also including a phase-change memory.

5. The circuit of claim 1 including a package containing stacked dice.

6. The circuit of claim 1 wherein said package is a folded stacked package.

7. The circuit of claim 2 wherein said first die includes a processor and a non-volatile memory.

8. The circuit of claim 1 including a non-volatile memory.

9. The circuit of claim 1 including a ball grid array package.

10. A method comprising:

providing a processor and a cross-point memory on separate dice; and

packaging said cross-point memory and said processor in the same package.

11. The method of claim 10 including packaging a volatile memory on a separate die in said package.

12. The method of claim 10 including packaging said processor and said cross-point memory in a folded stacked package.

13. The method of claim 10 including packaging a phase-change memory in said package.

14. The method of claim 10 including providing a bus on said die with said processor and coupling said processor to said cross-point memory through said bus.

15. The method of claim 10 including stacking said dice on top of one another.

16. The method of claim 10 including packaging a volatile memory in the same package with said processor and said cross-point memory.

17. The method of claim 10 including providing a ball grid array on said package.

18. A packaged integrated circuit comprising:

a first die including a processor; and

a second die including a cross-point memory.

19. The circuit of claim 18 including a third die with a volatile memory.

20. The circuit of claim 18 including a bus on said first die coupling said processor to said cross-point memory.

21. The circuit of claim 18 including a phase-change memory.

22. The circuit of claim 18 including a plurality of stacked dice.

23. The circuit of claim 18 including a folded stacked package.

24. The circuit of claim 18 including a ball grid array package.